Abstracts

A large-signal model of self-aligned gate GaAs FETs for high-efficiency power amplifier design

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A large-signal model which can simulate the power-added efficiency of p-pocket self-aligned gate GaAs MESFETs its proposed. This model includes a new drain current model and a gate bias dependent RF output resistance to express the drain conductance and its frequency dispersion at each gate bias. The simulated power-added efficiency agrees with the measured value with a maximum error of 5%. This model is also applicable to the distortion simulation by the introduction of new gate-source and gate-drain capacitance models using two variables for the gate and drain biases.

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